CISC-340 Digital Systems

Course Syllabus

Revised August 3, 2016

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Quick Reference

Course title: Digital Systems

Course number: CISC_340

Course dates: Monday, September 12, 2016 through Friday, December 2, 2016

Lecture Location: Dupuis Hall Room 217

Meeting day(s): Tuesday: 6:30 p.m. – 8:00 p.m. ; Thursday: 6:30 p.m. – 8:00 p.m. (90 minute classes)

Lab : Monday 8:30 – 10:30 / 11:30 – 13:30, Goodwin 248

Prerequisite(s): CISC-221 or equivalent

Instructor Information

- **Name:** Dave Dove
- **Email:** dove@cs.queensu.ca
- **Office location:** Goodwin Hall Room 753
- **Office hours:** Tuesday, Thursday 4 p.m.. - 6 p.m. (tentative)
- **Phone:** 533-6053

Teaching assistants: to be announced

Textbook: Digital Design. An Embedded System Approach Using VHDL.
Peter J. Ashenden
Morgan Kaufmann ISBN 978-0-12-369528-4

There is also extensive online material (queensu.brightspace.com).

Assessment:

*Note: The portion of your final course mark allotted to each of Individual Assessment, Team Assessment and Peer Assessment will be as follows:

Individual Work Assessment: 70% (*includes individual component of team projects)
Team Work Assessment: 20%
Peer Assessment : 10%

Individual Work Assessment (by Instructor)

- Quiz 1: 10%
- Quiz 2: 10%
- Quiz 3: 15%
- Quiz4: 15%
- Weekly Labs : 10%

- Individual Portion of 2 Team Projects: 10%

Total Individual Work Assessment: 70%

Consult the course web site for specific date information. Quizzes are 60 minutes in length and take place in the normally scheduled class period. All Quizzes are closed-book and no electronic devices are permitted (subject to review). There is no midterm or final exam.

Team Work Assessment (by Instructor)

- Team readiness (RAT) tests 6%
- Team in-class exercises 10%
- Assessment of Teamwork portion of 2 Team Projects * : 4%

*Project 1 will be completed in the first half of the term, Project 2 will be completed in the second half of the term.
The project assessments include both an individual component (~70%) and a teamwork component (~30%) of each project mark. This will effectively moderate the negative effects (in terms of assessment) caused by a non-performing team member.

It's important to understand that although the Team Assessment portion of your course mark is only 20%, the work that you do as a team may significantly affect your mark on individual Quizzes and also may affect your Peer Assessment mark.

Peer Assessment (by Students)

Assessment of your own team performance and the performance of your team members will be done at mid-term, and again at the end of the term. You must submit an assessment of your team members in order to receive a peer assessment mark. The mark you receive will be the average of the marks given to you by your team members (including yourself).

The assessment is submitted via a web form. The form will allow you to include comments that will be collated and sent to team members anonymously. Peer assessments have a rigid due date and time and submissions are not allowed after that.

Mid-term Peer Assessment 5%
End-of-term Peer Assessment 5%

Course Topics

1. Digital Circuit Basics
    - Basic electronics
    - Introduction to combinational logic
    - Boolean algebra theorems, truth tables, switching expressions
    - Implementation, simplification and customization
2. Design Tools

    - EDA(Electronic Design Automation) tools for design entry, simulation, synthesis, design management
    - Approaches to design verification
3. Combinational Systems
    - VHDL - A Hardware Description Language
        - VHDL Basics
    - Standard Combinational Modules
        - Gates, multiplexors, decoders, encoders, adders, ALUs
        - Example circuits relating to computer applications
4. Sequential Systems:
    - flip-flops, registers, state machines
    - State machine design, data vs control section design
    - Register Transfer Level (RTL) design of complex sequential systems
5. Communications
    - communications between chips, between chip and device, network communications
    - Interfacing common input and output devices.

Why Study Digital Logic in Computing Science?

1. A course on digital logic will include topics relating to performance and power consumption (important for mobile devices) not covered in courses about Computer Architecture.
2. A course on digital logic extends the study of abstraction layers of computers studied in Computer Architecture down into the lower layers of hardware implementation.
3. A course on digital logic helps explores the relationship between software and hardware.
4. A course on digital logic gives programmers more options in system design by making it feasible to include hardware design as part of the solution to system design problems. Programming language extensions are becoming available that allow the programmer to specify that code segments be implemented in hardware in embedded systems implemented with an FPGA (Field Programmable Gate Array). Sophistication of hardware design tools for FPGAs extends the ability to design hardware solutions beyond the exclusive domain of electrical engineers.
5. Use of FPGAs to implement real hardware designs remains relevant as a means of exploring computer theory and practice.
6. Concepts covered in digital logic design are compatible with recurring concepts in computing science such as dealing with complexity, the use of models, consistency and correctness, levels of abstraction, re-use of design elements, dealing with tradeoffs in time and space.

Course Learning Objectives:

Learning skills:

The delivery of this course is designed to develop and enhance self-learning and life-long learning skills:

- by adopting an inquiry-based learning approach.
- by making learning visible to the learner and to others.
- by frequent self-reflection on the learning process.

Communication skills:

The team-based, active learning delivery of this course provides the student opportunities to:

- Discuss and resolve in a team environment, case studies and issues relating to digital system design.
- Demonstrate your ability to articulate a technical position and support it with scholarly arguments.
- Demonstrate interpersonal and team interaction skills.

Content related skills:

In this course, you will individually, and as a team:

1. Design, implement, and verify the operation of simple digital circuits, using manual design, synthesis, and verification methods.
2. Model, design, simulate, and verify the operation of digital logic circuits using current EDA (Electronic Design Automation) software tools used by industry.
3. Create a RTL (Register Transfer Level) design of a complex digital logic function, starting with a model of the functional behaviour of a digital electronic circuit written in a high level programming language and ending with a functioning FPGA (Field Programmable Gate Array).
4. Evaluate and defend design choices relating to the distribution of hardware versus software implementation to satisfy speed, complexity, and labour criteria.
5. Interface common sensors, switches, display devices, and servo motors to an embedded processor.

Course Outcomes:

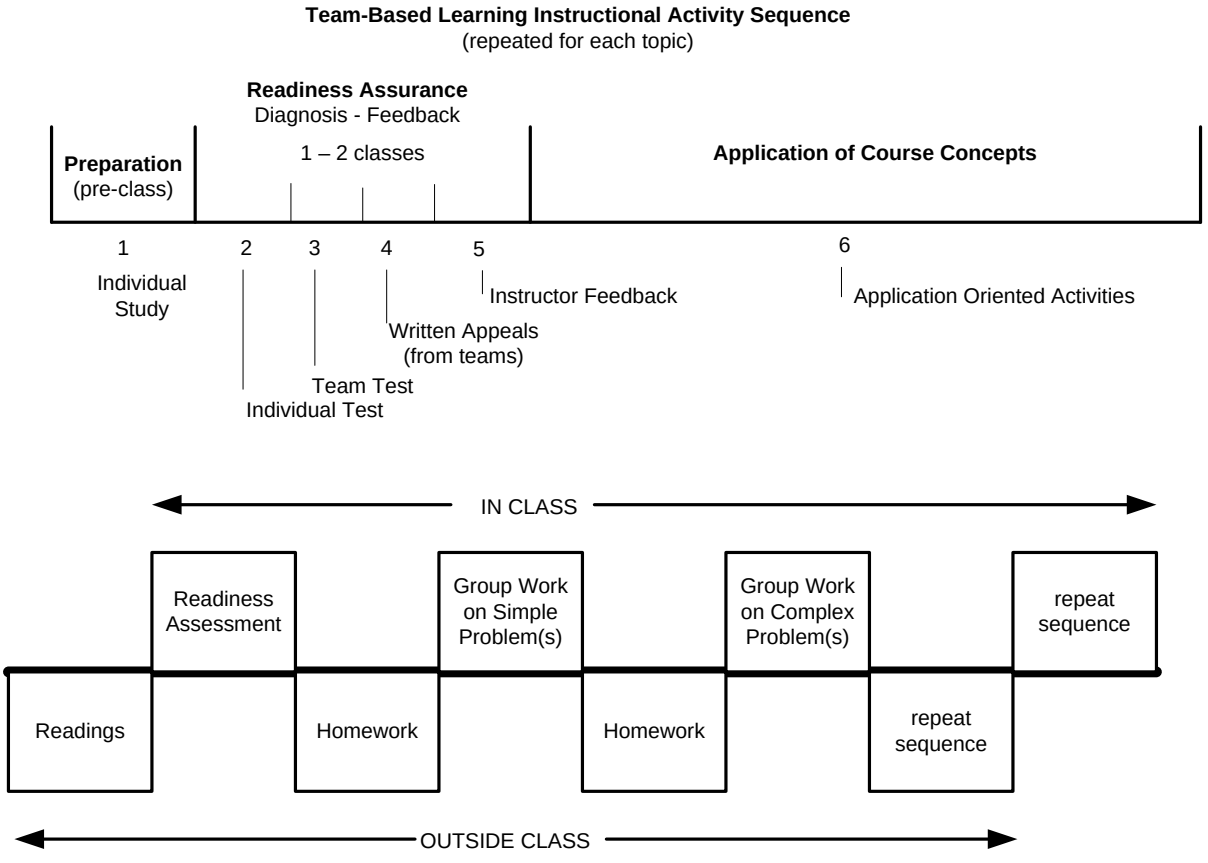
Your success will be measured in these ways:

1. Assessment of preliminary multiple choice quizzes, both individually and as a team, relating to concepts covered in reading assignments that precede major topics (Readiness Assessment Tests).
2. Assessment of in-class team- based exercises.
3. Assessment of two, team-based projects.
4. Assessment of individual in-class quizzes consisting of multiple choice and short answer questions given approximately every three weeks (4 per term).
5. Peer assessment of your work as a team member.

Course Delivery

This course will use a team-based, active learning approach for course delivery. In this approach, the focus is on what the learner learns rather than on what the instructor teaches. Course content is acquired by the learner under the guidance of the instructor. The instructor will give a brief overview of the topic. Students will be given a reading/research assignment that covers the topic and includes basic questions and possibly sample problems with solutions. Students will then be tested on basic comprehension of what they have read, both individually and then as a team. Team solutions will be discussed and problem areas addressed, possibly with a short lecture from the instructor. The remainder of class time for the topic will be used to present problems and have teams develop, present, and discuss solutions. In preparation for in-class work, students may be required to complete out-of-class assignments. This approach to learning involves active participation of the students as most of the class time is spent applying course concepts and receiving immediate feedback on the student's level of understanding.

During the first class of the term, permanent teams of about 6 – 8 students will be formed of students with diverse qualifications. These teams will sit together in class and take part in team based discussions, in-class activities and team projects.



1st class of a topic

A multiple choice, Readiness Assurance Test (RAT) will be given individually. Then, the team will get together and discuss what the answers should be. The purpose of the individual RAT is to prepare the student for the subsequent team discussion about the material for the team RAT that immediately follows. The team will submit answers to the same test with immediate feedback as to whether their answers were correct or not. Team answers are submitted and contribute to course assessment. If a team feels strongly about the correctness of their answer but it is marked wrong, there is an appeal process available to them. The individual tests are submitted but do not normally count towards a course mark. An individual's credit for the team answers may be revoked if there is a pattern of low readiness or absenteeism.

The purpose of the RATs is to ensure that students are adequately prepared for the subsequent class activities on the current topic and to identify common areas of difficulty relating to the topic which are then discussed and clarified.

2nd class of a topic:

Any remaining questions about the topic are discussed. Problems relating to current topic are presented. All teams work on the same problems. Team solutions are compared and discussed. Solutions are submitted for marking.

3rd and subsequent classes of a topic:

Additional problems may be presented and solved.
Any unresolved problem areas with the topic are dealt with.
A short overview of the next topic is given.

There will be two peer assessments of your work as a member of a team. The first will be mid-term and the second will be at the end of the term. The assessments will be done by the other members of your team. Assessments will be submitted online and comments subsequently passed anonymously to individual team members.

Academic Integrity

Academic integrity is constituted by the five core fundamental values of honesty, trust, fairness, respect and responsibility (see www.academicintegrity.org). These values are central to the building, nurturing and sustaining of an academic community in which all members of the community will thrive. Adherence to the values expressed through academic integrity forms a foundation for the "freedom of inquiry and exchange of ideas" essential to the intellectual life of the University.

Students are responsible for familiarizing themselves with the regulations concerning academic integrity and for ensuring that their assignments conform to the principles of academic integrity. Information on academic integrity is on the Arts and Science website (see http://www.queensu.ca/artsci/academics/undergraduate/academic-integrity), and from the instructor of this course. Departures from academic integrity include plagiarism, use of unauthorized

materials, facilitation, forgery and falsification, and are antithetical to the development of an academic community at Queen's. Given the seriousness of these matters, actions which contravene the regulation on academic integrity carry sanctions that can range from a warning or the loss of grades on an assignment to the failure of a course to a requirement to withdraw from the university.

Copyright of Course Materials

The material on this website is copyrighted and is for the sole use of students registered in CISC-340. The material on this website may be downloaded for a registered student's personal use, but shall not be distributed or disseminated to anyone other than students registered in CISC-340 during the current term. Failure to abide by these conditions is a breach of copyright, and may also constitute a breach of academic integrity under the University Senate's Academic Integrity Policy Statement.

Absenteeism

In a team-based learning environment, it is vitally important for you to attend every class.

Individual attendance is recorded during classes involving in-class exercises. If the team and instructor was not given prior notice of an impending absence and the reason for it, the absent student will not get credit for the team activity. If a student is absent a significant number of times without giving the team notice or team members have doubts about the validity of reasons for absenteeism, it may affect their peer evaluation of that student. If you will be missing a significant number of classes, you need to discuss this with an instructor to make appropriate assessment modifications.

Students who miss a Readiness Assessment Test will not get team credit for it unless the instructor has been previously informed of the absence and the reason for it.

Students who miss a Quiz must inform the instructor before or on the day of the Quiz of the reason for the absence and may be given a single opportunity to write a makeup Quiz.

If you are the student who is responsible for bringing in a laptop and/or parts kit for in-class activities, it is crucial that arrangements be made with another student to bring in the parts kit and an alternate laptop for in-class activities and inform the instructor of your impending absence. Otherwise your team will not be able to do any work that day and will not get any credit for it.

Policies

- Teams will be provided microcontroller boards and associated electronic parts that will be used in team projects and some class activities.
- Labs are held in Goodwin Hall Room 248.
- Lab work can be done on any PCs in the CASLAB domain. Login to the CASLAB domain and create files on your personal "Z:" drive.
- Students can download the required FPGA software from the Xilinx web site. You will find download links on the Extras page of the course web site. Students may do the all of the project

work on their own PCs if they wish, subject to how and where teams decide to meet to work on the projects. Other software resources will be made available as required.

- Late labs and project documentation will not be accepted without prior arrangement with the course instructor. Late submissions must be made to the course instructor or the general office in order to be accepted. Anything slipped under my door (Goodwin 753) will be disposed of.
- Note that there is no Mid-Term or Final Exam in this course.

Team Projects

Team projects will use Xilinx Vivado EDA software. It is installed in Goodwin 248, and Walter Light 310. This software is free and available online. Download the Xilinx Vivado Web Edition software at http://www.xilinx.com. Additional (free) software components may be required and will be made available as required. Both projects will include individual and team presentations to the class relating to their projects.

- Project #1 Embedded system with I/O interfaces. Investigation of switches, sensors, motors, and displays.
- Project #2 Embedded system focusing on the IOT (Internet of Things).

Peer Assessment

The students in each team will assess the other students in their team twice during the term – at mid-term and at the end of the term. The assessment is done via a web-based form.

Comments on the other students of the team are forwarded to the students as anonymous comments.