CISC422/853: Formal Methods in Software Engineering: Computer-Aided Verification



Topic 7: Specifying, or

How to Describe How the System Should (or Should Not) Behave

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Readings:

- Spin book: Chapter 4 (Defining Correctness Claims), Chapter 6 (Automata and Logic)
- · Course notes on CTL

Outline

- Formal specifications
- Types of formal specifications:
 - assertions
 - invariants
 - safety and liveness properties
- How to express safety properties:
 - FSAs, regular expressions, Never Claims
- How to express liveness properties:
 - progress labels, Buechi Automata, Never Claims, Linear Temporal Logic, Computation Tree Logic
- How to manage the complexity of specifications:
 - specification patterns

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(Formal) Specifications

- What is a specification?
- What is a formal specification?
- Properties of good formal specifications?
 - As precise and detailed as necessary, and as abstract (i.e., unconstraining) as possible
 - Consistent
 - Correct (internally, externally)
- Why use formal specifications?
 - Unambiguous
 - · Sometimes more succinct
 - Amenable to automatic analysis

Observables

- "Atomic propositions" used in a specification
- In BIR
 - global and local variables (in their scope)
 - existential (anonymous) thread program counter Property.existsThread(t, loc5)

In PROMELA

- · global and local variables
- end-states, progress states, and accept states
 - $^\circ~$ needed for expression of liveness (progress) properties
 - E.g., non-progress through reserved boolean variable np_ (false in s iff at least one process is at a control flow state marked with a progress label)
 - ° more on these later
- process ids through reserved variable __pid CISC422/853. Winter 2009 Specifying

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Types of Formal Specifications for Assertions Concurrent and Reactive Systems Assertions Express a property of observables at particular **Example:** location Invariants thread T() { Most basic formal specification; already used by Safety properties ... John von Neumann in 1947 loc loc7: Liveness properties In BIR and Promela: assert(b); when b do { What kind of correctness claim does an assertion . . . make, that is, what does it mean if there is assert(x > y) no assertion violation?: "No matter along which path control has reached the location of the assertion, the boolean expression in the assertion evaluates to true at that location" • an assertion violation?: "There is at least one execution such that the boolean expression in the assertion does not evaluate to true at that location" CISC422/853. Winter 2009 5 CISC422/853, Winter 2009 Specifying Specifying

Example 1: Simple Race Condition

<pre>byte state = 1; active proctype A() { (state == 1) -> state++; assert(state == 2) } active proctype B() { (state == 1) -> state; assert(state == 0) }</pre>			
<pre>\$ spin -a simple.pml \$ gcc -o pan pan.c \$./pan -E</pre>			
<pre>\$ spin -t -p simple.pml 1: proc 1 (B) line 7 "simple.pml" (state 1) [((state==1))] 2: proc 0 (A) line 3 "simple.pml" (state 1) [((state==1))] 3: proc 1 (B) line 7 "simple.pml" (state 2) [state] 4: proc 1 (B) line 8 "simple.pml" (state 3) [assert((state==0))] 5: proc 0 (A) line 3 "simple.pml" (state 2) [state++] spin: line 4 "simple.pml", Error: assert(on violated spin: text of failed assertion: assert((state==2))</pre>			

[Source: spinroot.com]

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Example 2: Checking Mutual Exclusion Using Assertions

- Does protocol below ensure mutual exclusion and deadlock freedom?
- How can we check this using Bogor or Spin?

system MuxTry { boolean flag1; boolean flag2;	
<pre>thread T1 () { loc loc0: do {flag1 := true; } goto loc2;</pre>	<pre>thread T2 () { loc loc0: do {flag2 := true; } goto loc2;</pre>
loc loc2: when (!flag2) do {} goto loc3;	loc loc2: when (!flag1) do {} goto loc3;
loc loc3: do {} goto loc4;	loc loc3: do {} goto loc4; critical regions
loc loc4: do {flag1 := false; } goto loc0; }	loc loc4: do {flag2 := false; } goto loc0; }
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Example 2: Checking Mutual Exclusion Using Assertions (Cont'd)

To check mutual exclusion, instrument protocol as follows:

system MuxTry { boolean flag1; boolean flag2; int c;	
thread T1 () {	thread T2 () {
loc loc0:	loc loc0:
do {flag1 := true;} goto loc2;	do {flag2 := true; } goto loc2;
loc loc2:	loc loc2:
when (Iflag2) do {} goto loc3;	when (!flag1) do {} goto loc3;
<pre>loc loc3: do {c := c+1; assert(c==1);} goto loc4;</pre>	loc loc3: do {c := c+1; assert(c==1); } goto loc4; critical regions
loc loc4:	loc loc4:
do {c := c-1; flag1 := false;}	do {c := c-1; flag2 := false; }
goto loc0;	goto loc0;
}	}

What about deadlock freedom?

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Assertions in Java

- Java 1.4 also supports assertions
- What does it mean if a Java assertion is
 - violated?
 - not violated?
- What's the difference between assertions in Bogor/Spin and Java?

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Invariants

- Express property of observables that holds at every location
- What kind of correctness claim does an invariant make, that is, what does it mean if there is
 - no invariant violation?:
 - "At all locations along all executions of the system, the property holds"
 - an invariant violation?:
 - "There is at least one location along an execution such that the property does not hold at that location"
- How do invariants compare to
 - · assertions?
 - "loop invariants" in Hoare Logic?

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Multiplication Example

Consider a simple program with a loop invariant

```
// assume parameters m and n
count := m;
output := 0;
// loop invariant: m * n == output + (count * n)
while (count > 0) do {
    output := output + n;
    count := count - 1;
}
```

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Multiplication Example

BIR Version:

system Mult { int m: thread T1 () { int n: loc loc0: int count; int output; main thread Main () { goto loc0; loc loc0: **do** {m := (int (0,255)) 5; return; n := (int (0,255)) 4;count := m: output := (int (0,255)) 0;start T1(); } return;

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when (count == 0) **do** {}

Remember: No interleaving between these two

assignments!

Now, ... how to program the check of the invariant? [Source: CIS842 @ KSU] 13

Checking Invariants

• To check invariant / on a program with the threads

Main, T1, ..., Tn add an assertion of / as the last transition of *Main*:

- Why does this work?
 - Model-checker will explore all possible interleavings between *Main* and each *Ti*

· Thus, the assertion statement will get interleaved (on some trace) between every pair of execution steps of each Ti and thus checking the invariant on every state along every possible execution of T1, ..., Tn

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[Source: CIS842 @ KSU] 14

Multiplication Example: Checking Invariants

	system Mult {		thread T1 () {	
	 main thread Main () { loc loc0: do {m := (int (0,255)) 5; n := (int (0,255)) 4; count := m; output := (int (0,255)) 0; start T1(); } goto loc1;		<pre>loc loc0: when (count > 0) do { output := output + n; count := count - 1; } goto loc0; when (count == 0) do {} return; }</pre>	
	<pre>loc loc1: do {assert (m*n == output+(count*n));} return; }</pre>	d	[Source: CIS842 @ KSUI] 15	
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Checking Invariants



In other words, there exists a path where we do 0 steps of T1 then check *I*, there exists a path where we do 1 step of *T1* then check *I*, there exists a path where we do 2 steps of T1, then check I, etc.

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main thread Main () ... loc locAssert: do {assert (I);} return:



Assertions and Invariants

- Assume location I in t can be characterized by pt at I.
 - Then, checking for assertion q at I in t is equivalent to checking the invariant p_{t at I} -> q



Safety and Liveness: Informally

Consider the mutual exclusion problem again:

proctype T1() {	proctype T2() {
do	do
:: // non-critical region	:: // non-critical region
// entry protocol	// entry protocol
// critical region	// critical region
// exit protocol	// exit protocol
od;	od;

Reg1: "Both processes are never in their critical region at the same time"

Safety and Liveness: Informally (Cont'd)

A trivial solution?!

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proctype T1() {	proctype T2() {
do	do
:: // non-critical region	:: // non-critical region
(false); // entry protocol	(false); // entry protocol
// critical region	// critical region
skip; // exit protocol	skip; // exit protocol
od;	od;

Reg1: "Both processes are never in their critical region at the same time"

Reg2: "After starting its entry protocol, a process will always eventually be allowed into its critical region"

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Safety and Liveness: Informally (Cont'd)

Safety	Liveness
Intuitively: "something bad never happens" Examples: "x is always positive" "The system never deadlocks" "The elevator will always be between the first and third floor" "The system will terminate after 10 steps"	Intuitively: "something good eventul happens" Examples: "x will eventually be pos "The system will termina" "After pressing the require button, the elevator will eventually appear"
Terms due to Leslie LamportWhat about assertions and invariar	nts?

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ituitively:
"something good eventually
happens"
xamples:

- sitive"
- ate"
- iest

Safety and Liveness: Formally

"Once the 'bad thing' has occurred, there's no recovering from it"
•
"It is always possible
to happen"
"Safety and liveness
are fundamental notions"

Safety and Liveness: Formally (Cont'd)



Safety and Liveness: More Examples

- Reg 1: "A use of a variable must be preceded by a declaration"
- Reg 2: "When a file is opened, it must subsequently be closed"
- Reg 3: "You cannot shift from 'drive' to 'reverse' without passing through 'neutral' "
- Reg 4: "No pair of adjacent dining philosophers can be eating at the same time"
- Reg 5: "Never two processes in their critical region at the same time"
- Reg 6: "Every philosopher will always eat eventually"

Which requirements are safety properties and which are liveness properties? CISC422/853, Winter 2009 Specifying 24

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Safety, Liveness, and Run-time Monitoring

Theorem: Every property over finite traces is a safety property

 \Rightarrow Any property that a run-time monitor can check is a safety property



How to Express Safety and Liveness Properties?

Safety

- assertions and invariants
- FSAs
- · Regular Expressions
- Never Claims

Liveness

- · progress labels
- · Buechi automata
- Never Claims
- Linear Temporal Logic (LTL)

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FSAs for Safety Properties

• S = "Every file is opened before reading, writing, or closing"



what we want to happen

■ ¬S = "A read, write, or close happened before an open" (violation)



what we don't want to happen Model checkers look for violations, so they typically expect violations of the safety property to be specified

Specifying Safety Properties in Bogor

extension Property for edu.ksu.cis.projects.bogor.ext.lite.property.Property { expdef boolean transformation(string, string); }

```
function FSASpec() {
    loc init: live {}
      when Property.transformation("MAIN", "open") do { } goto opened;
      when Property.transformation("MAIN", "close") do { } goto bad$State;
      loc opened: live {}
      when Property.transformation("MAIN", "open") do { } goto bad$State;
      when Property.transformation("MAIN", "close") do { } goto init;
      loc bad$State: live {} // bad state
           do { } goto bad$State;
    }
```

What's the property specified here?

Observables, Again

- Alphabet Σ contains the "observables", i.e., the atomic propositions over which the specification is phrased
- Checker must be able to determine whether or not an observable is true in a given state
 - may be able to determine directly (e.g., variable values)
 ° E.g., x>3 or np_ in Spin
 - if not, helper variables and assignments must be used. E.g.:
 - ° fileOpen := true;
 - $^{\circ}\;$ count number of processes in critical region
- In Bogor:
 - · Observable: Values of variables and program counters
 - · Not observable: e.g., ids of enabled threads

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Regular Expressions (Recap)

 Let Σ be the alphabet Regular expressions over Σ are built as follows: Every a∈Σ is a regular expression over Σ • If e, e_1 , e_2 are regular expressions over Σ , then ° e₁; e₂ concatenation/sequencing $\circ e_1 | e_2$ choice/disiunction ° e* reflexive and transitive closure/iteration with 0 ° (e) grouping ° e? option ° e+ transitive closure/iteration without 0 derived any symbol/don't care ° [e₁, e₂, ...] union/multiple disjunction ° [- e₁, e₂, ...] complement/exclusion also are regular expressions over Σ Every regular expression e over Σ defines a set of words over Σ, that is, L(e) $\subseteq \Sigma^*$

 $\begin{array}{c} \text{Inat IS, L(e)} \subseteq \Sigma\\ \text{CISC422/853, Winter 2009} \end{array}$ Specifying

Regular Expressions

Theorem:

- For every FSA A, there exists a regular expression e_A, such that L(A) = L(e_A).
- For every regular expression e, there exists an FSA A_e, such that L(e) = L(A_e).
- \Rightarrow FSAs and regular expressions can be used interchangeably
- \Rightarrow So, if FSAs can be used to express safety properties, then regular expressions can, too

Regular Expressions (Cont'd)

- Example:
 - Let open, close $\in \Sigma$
 - positive:
 - ° "Every open is immediately followed by a close"
 - ° ([- open]* (open close)?)*
 - negative:
 - ° "At least one open is not immediately followed by a close"
 - ° (.)* open ([- close] (.)*)?

Never Claims: FSAs in Spin

- Used in Spin to express violations of
 - · safety properties, and
 - liveness properties (more on this later)
- For the moment, we can think of a Never Claim as
 - a Promela program that defines an FSA
 - expressing how a safety property can be violated, that is, the negation of a safety property never {



Never Claims



- NC executed synchronously (remember?) with system
- Matching a never claim NC:
 - A run t matches NC, if t causes NC to
 - be fully executed, that is, the outermost "}" of the claim to be reached, or
 - $^\circ\;$ reach an acceptance cycle
 - NC specifies behaviours that should never occur. So, if run t matches NC, we have found a violation!

• Not matching a never claim NC:

- If the run t does not match NC, then t is ok, because it does not exhibit the violating behaviour described by NC
- Note that if run t causes the NC to "get stuck" (i.e., NC has no enabled transition and t is not done), then t does not match NC CISC422/853, Winter 2009 Specifying 34



never {

Never Claims (Cont'd)

"access operations are used in proper order"

There's an implicit acceptance cycle at the end of every never claim. So, the following two claims are equivalent:

```
do
                                          never {
        :: open -> do
                                                   do
                   :: close -> break
                                                   :: open -> do
                   :: else -> skip
                                                              :: close -> break
                   od
                                                              :: else -> skip
        :: else -> break
                                                              od
        od
                                                   :: else -> break
accept: do
                                                   od
        :: true -> skip
                                          }
        od
```

Never Claims (Cont'd)

- Can contain all of Promela's control-flow constructs
 - e.g., if, do, goto, etc
- Should be side-effect free (not change the state of the system being analyzed), that is, should only contain expression statements
- Can be non-deterministic



All of these can be used to check that "*x* is never 13"! Why?

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```

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Expressing Liveness Properties

- Want to say that something good always eventually happens,
 i.e., that system always eventually makes some progress
- Violation: Execution along which eventually no more progress (towards the good thing) is made
- 3 possibilities to express liveness property in Spin:
 - 1. using progress labels (for simple liveness properties)
 - 2. using Buechi Automata (for simple and complex liveness properties)
 - 3. using Linear Temporal Logic (LTL) (for simple and complex liveness properties)
- Assumption: system has only infinite executions (possibly use "stutter extension")

```
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```

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1. Using Progress Labels

- Simple idea: label certain states as "good", i.e., as progress states
 - e.g., Philosopher1.eating
- Claim with respect to system S and progress state s:
 - From all reachable states in S, eventually s will always be reached

 \Rightarrow s occurs infinitely often along all executions of S

- Violation:
 - There is an execution in S along which s occurs only finitely many times
 - \Rightarrow There is a run in S that's either 1) finite, or

2) ending in a cycle not containing s (non-progress cycle)

If we add self-loops to all states

with no outgoing arcs (stutter extension),

1) can be reduced to 2) CISC422/853, Winter 2009 Specifying

Stutter Extension

- Goal: When detecting non-progress cycles, don't want to have to distinguish between finite and infinite execution
- Solution:
 - Let M be an iFSA
 - We define "stutter extension" of M stutter(M) = (M.S, M.S₀, L', δ', M.F)

where

- $L' = M.L \cup {\text{"idle"}}$
- $\delta' = \mathsf{M}.\delta \cup \{(\mathsf{s}, \text{``idle''}, \, \mathsf{s}) \mid \mathsf{s} \in \mathsf{M}.\mathsf{S} \land \mathsf{s} \text{ has no outgoing transitions} \}$
- And then use stutter(M) to look for non-progress cycles

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Non-Progress Cycles in Spin



compile verifier with –DNP and run it with –I:

\$ gcc -DNP -o pan pan.c

\$./pan -1 CISC422/853, Winter 2009 Specifying

or select

"Non-Progress Cycles" in "Basic Verification Options" in xspin

2. Using Buechi Automata

- Progress labels alone are not enough to express more complicated liveness properties such as
 - S = "The first open is always eventually followed by a close"
- Violation:
 - $\neg S =$ "The first open is never followed by a close"



• Ok. but:

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because only finite words can be accepted by FSA

\rightarrow need to change acceptance condition of FSA

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ω-Acceptance

An accepting ω -run of an FSA A is an ω -run $\sigma = (s_0, l_0, s_1)(s_1, l_1, s_2)(s_2, l_2, s_3)...(s_{i-1}, l_{i-1}, s_i)...$ of A such that \exists s_f \in A.F. "s_f occurs infinitely often in σ ".

Example:

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(block unblock))ω

Buechi Automata

An Buechi automaton is a FSA with ω-acceptance.

Buechi automata are sometimes also called oautomata

Buechi Automata for Liveness: Example 2

Let's try another liveness property

Specifying

- S₂ = "Every open is always eventually followed by a close"
- Violation:
 - $\neg S_2 =$ "At least one open is never followed by a close"



Used to overread initial occurrences of 'open' that are followed by a close

For example:

open [- close]^{ω} $\subseteq L^{\omega}(A_{\neg S_{\alpha}})$ open close open [- close] $\bar{\omega} \subseteq L^{\omega}(A_{\neg S_{\alpha}})$ Note: other solutions are possible! Which?

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open read^{ω} \notin L(A_{-s})

Buechi Automata for Liveness: Example 2 (Cont'd)

- Let's try another liveness property
 - S₂ = "Every open is always eventually followed by a close"
- Violation:
 - $\neg S_2 =$ "At least one open is never followed by a close"
- Why doesn't A' capture ¬S₂?









- Never claims are Buechi automata!
- Remember: run t is accepted/ matched by never claim NC, if t causes NC
 - · to end in an acceptance cycle, or
 - to be fully executed (implicit acceptance cycle)
- Example:
 - S₂ = "Every open is always eventually followed by a close"
 - word $w \in L^{\omega}\!(A_{\neg S2})$ iff w matches $NC_{\neg S_2}$

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Temporal Logic



3. Using Linear Temporal Logic (LTL)



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"x!13 in every state in every run of M"

Linear Temporal Logic (LTL) (Cont'd)



Formal Semantics of LTL

- We now want to define precisely when an LTL formula ϕ holds for some iFSA M
- Problem: LTL formulas are interpreted over infinite runs not finite ones
- Solution:
 - Let M be an iFSA
 - We define "stutter extension" of M stutter(M) = (M.S, M.S₀, L', δ ', M.F)
 - where
 - $L' = M.L \cup \{\text{``idle''}\}$
 - $\delta' = M.\delta \cup \{(s, "idle", s) \mid s \text{ has no outgoing transitions in M} \}$
 - And interpret LTL formulas over L^ω(stutter(M))

As before

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Formal Semantics of LTL

Linear Temporal Logic: Examples 1

- Let M be iFSA, ϕ be LTL formula Note implicit universal $M \models \phi$ iff $\forall r \in L^{\omega}(stutter(M))$. $r \models \phi$ quantification over all paths where ■ r⊨p iff eval(s_0, p) = true • $\mathbf{r} \models \phi_1 \land \phi_2$ iff $\mathbf{r} \models \phi_1$ and $\mathbf{r} \models \phi_2$ iff r₁⊨ø ■ r⊨Xo ■ r⊨Gø iff $\forall i \ge 0$. $r_i \models \phi$ iff $\exists i \geq 0$. $r_i \models \phi$ ■ r⊨Fo • $r \models \phi_1 \cup \phi_2$ iff $\exists i \ge 0$. $r \models \phi_2$ and $\forall 0 \le k \le i$. $r \models \phi_2$ where r is assumed to be of the form $s_0s_1s_2...$ and For every state s and $r_i = s_i s_{i+1} s_{i+2} \dots$ for all $i \ge 0$ and eval: $M.S \times AP \rightarrow \{true, false\}$ p, we have a way of
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every atomic proposition determining if p holds in s

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LTL Equivalences

- all propositional equivalences, e.g., $\neg \neg \phi \leftrightarrow \phi$
- $\left.\begin{array}{ccc} \neg G\phi & \leftrightarrow & F\neg\phi \\ \hline \neg F\phi & \leftrightarrow & G\neg\phi \end{array}\right\} G and F are duals$ $\left.\begin{array}{ccc} G\phi & \leftrightarrow & \phi \land X G \phi \\ \hline F\phi & \leftrightarrow & \phi \lor X F\phi \end{array}\right\} use X to "unroll"$
- $\phi_1 \cup \phi_2 \quad \leftrightarrow \quad \phi_2 \vee (\phi_1 \wedge X(\phi_1 \cup \phi_2))$
- true U $\phi \leftrightarrow F\phi$

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Linear Temporal Logic: Examples 2

- $(X \times open) \rightarrow (X \times X \times close)$
 - "Along all runs, if there's an 'open' in the second state, then there is a 'close' in the fourth state"
- G (open \rightarrow F close)
 - "Along all runs, it must always be the case that an 'open' is eventually followed by a 'close'"
- FG p
 - "Along all runs, it must eventually be the case that p always holds"
 - Example of a run satisfying/violating the specification?
- GF p
 - "Along all runs, it must always be the case that eventually p holds", aka, "p holds infinitely often"
 - · Example of a run satisfying/violating the specification?
- G((rainStart $\land \neg$ rainEnd \land F rainEnd) \rightarrow (roofClosed U rainEnd))
 - "Once the rain has started, the roof remains closed until the rain ends"

• "The roof is always closed while it rains" CISC422/853, Winter 2009 Specifying

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LTL Notes

- Just like Buechi Automata, LTL can be used to express both
 - safety properties, e.g., G x!=13, and
 - liveness properties, e.g., F x=0
- Invented by Prior (1960's)
- First used to reason about concurrent systems by Amir Pnueli (Turing Award Winner)

LTL Notes (Cont'd)

- LTL's universal path quantification
 - An LTL formula is implicitly universally quantified over all paths of the system:

 $M \vDash \phi$ iff $\forall r \in L^{\omega}(stutter(M))$. $r \vDash \phi$

 How do you express that there exists a path satisfying a certain property \$\phi\$? Hint: Remember Assignment 1!

Never Claims versus LTL

- Never Claims (= Buechi Automata) are strictly more expressive:
 - $^\circ\,$ Anything expressible in LTL can be expressed with a Never Claim
 - $^\circ~$ Not everything expressible with a Never Claim is expressible in LTL
 - Example: e may be received after an even # of transitions and e is never received after an odd # of transitions

G, F, and U

F is special case of U

LTL and Buechi Automata

Theorem: For any LTL formula ϕ , there exists a Buechi automaton A_{ϕ} that accepts those runs for which ϕ is satisfied, i.e., $\forall \phi. \exists A_{\phi}. L(A_{\phi}) = \{r \mid r \vDash \phi\}$

Examples: The LTL formula

- 1. G p corresponds to which Buechi automaton?
- 2. FG p corresponds to the Buechi automaton:

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3. GF $\neg p$ ($\neg p$ holds infinitely often) corresponds to Buechi automaton:



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LTL and Spin

 Can use Spin to generate Buechi automaton (Never Claim) corresponding to a given LTL formula:



LTL and Spin (Cont'd)

🗙 SPIN CONTROL 4.2.6 27	🗙 Linear Time Temporal Logic Formulae	
File Edit View Run	H Formula: 🗇 done	Load
#define MAX 10	Operators: [] \diamond U \rightarrow and or not	
byte x=0;	Property holds for: $igstarrow$ All Executions (desired behavior) \bigcirc No Executions (error behavior)
proctype P(chan in, out)	Notes:	
byte y;	🛆 Use Load to open a file or a template.	
do		
tif		
:: else -> break	Symbol Definitions:	
fit	A #define done (x==10)	
10/9; x = u+1		
od Ö		
8		
proctype Q(chan in, out)	Never Claim:	Generate
{ 	A never { /* !(◇ done) */	
bute ut	accept_init:	
	if	
do	:: (! ((done))) -> goto T0_init	
y = x+1;	1, f1;	
A) Instru		
+ spin -a -X -N pan.ltl p	ar Verification Result: valid	Run Verification
– gcc -w -o pan -D_POSIX_S	\square A parning for p.g. reduction to be valid the never claim must be stutter-iv	ouariant
time /pan -v -X -m10000	(never claims generated from LTL formulae are stutter-invariant)	Tool Tollio
Nor in reaction done/	depth 0: Claim reached state 3 (line 57)	
17 A COLORED OF	(Spin Version 4.2.5 27 Uctober 2005) + Partial Order Reduction	

LTL and Spin (Cont'd)

- xspin has LTL property manager
 - edit, store, load LTL properties
 - · view them as never claims
- Checking system S wrt LTL formula φ in Spin

("Does S satisfy ϕ ?"):

- Spin computes $NC_{\neg\phi}$, i.e., Never Claim of negation of ϕ
- Spin explores state space of $S \otimes NC_{\neg_{0}},$ i.e., the synchronous composition of S with $NC_{\neg_{0}}$
- If $S \otimes NC_{\neg \phi}$ has run ending in acceptance cycle, then ° "Violation!"
 - $^\circ~$ S can exhibit behaviour violating ϕ and output counter example
- If $S{\otimes}NC_{\neg_{\varphi}}$ has no run ending in acceptance cycle, then
 - ° "No violation!"
 - $^\circ~$ S cannot exhibit behaviour violating ϕ

Summary

- (Formal) Specifications
- Types of formal specifications
 - · assertions
 - invariants
 - safety and liveness properties
- How to express safety properties
 - FSAs and regular expressions
 - Never Claims

• LTL

- How to express liveness properties
 - · progress labels
 - Buechi Automata and Never-Claims

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• LTL

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how to check them using Bogor and Spin

how to check them using Spin

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Summary (Cont'd)

Bogor

 checks for violations of safety properties expressed using assertions, invariants, or FSAs (expressed in BIR)

does not check for liveness properties

Spin

- checks for violations of liveness properties expressed using
 - ° progress labels: "Is there a run not ending in a progress cycle?"
 - Buechi Automata (expressed as Never Claims): "Is there a run that fully matches the Never Claim?"
 - LTL formulas (expressed as Never Claims): "Is there a run that fully matches the Never Claim representing the negated LTL formula?"

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Computation Tree Logic (CTL) (1)



Computation Tree Logic (CTL) (2)

Temporal operators in CTL have the following form

PathQuantifier StateQuantifier

where

- PathQuantifier ∈ {All, Exists}
- StateQuantifier ∈ {Globally, Finally, neXt, Until}

CTL formulas are defined by the following BNF

As before, $p \in AP$, that is, p is an atomic proposition

Computation Tree Logic (CTL) (3)

CTL formulas are defined by the following BNF

$arphi \ ::=$ path quantifier	$\begin{array}{l c c c c c c c c c c c c c c c c c c c$	
$AX \varphi$	"Along all paths, in the next state, φ holds"	
$\mathbf{EX} \varphi$	"Along at least one path, in the next state, φ holds"	
AG φ	"Along all paths, in all future states, φ holds"	
	"Along all paths, φ holds globally"	
$EG \varphi$	"Along at least one path, in all future states, φ holds"	
	"Along at least one path, φ holds globally"	
$\mathbf{AF} \ \varphi$	"Along all paths, in some future state, φ holds", or	
	"Along all paths, φ holds eventually"	
state $~{ m EF}~arphi$	"Along at least one path, in some future state, φ holds", or	
quantifier	"Along at least one path, φ holds eventually"	
$A \left[\varphi_1 \ U \ \varphi_2 \right]$	"Along all paths, φ_1 holds at least until φ_2 does"	
$\mathrm{E}\Big[arphi_1 \mathrm{~U~} arphi_2\Big]$	"Along at least one path, φ_1 holds at least until φ_2 does"	
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Computation Tree Logic (CTL) (4)

Consider following computation tree



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Computation Tree Logic (CTL) (5)



Computation Tree Logic (CTL) (6)



CTL Semantics

Formulas are interpreted over interpreted finite state machines. Given an iFSA $M = (S, S_0, L, \delta, F)$, a state s, and a CTL formula φ , the satisfaction relation $(M, s) \models \varphi$ is defined to be the smallest relation that satisfies:

 $(M,s) \models tt$

- $(M,s) \models p \text{ if } eval(p,s) = true$
- $(M,s) \models \neg \varphi_1 \text{ if not } (M,s) \models \varphi_1$
- $(M,s) \models \varphi_1 \land \varphi_2$ if $(M,s) \models \varphi_1$ and $(M,s) \models \varphi_2$
- $(M,s) \models \varphi_1 \lor \varphi_2$ if $(M,s) \models \varphi_1$ or $(M,s) \models \varphi_2$
- $(M,s) \models \varphi_1 \rightarrow \varphi_2$ if not $(M,s) \models \varphi_1$ or $(M,s) \models \varphi_2$

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- $(M, s) \models \mathbf{AX} \varphi$ if for all s' such that $(s, l, s') \in \delta$ for some $l \in L$, we have $(M, s') \models \varphi$
- $(M,s) \models \mathbf{EX} \varphi$ if for some s' such that $(s, l, s') \in \delta$ for some $l \in L$, we have $(M, s') \models \varphi$
- $(M, s) \models \mathbf{AG} \varphi$ if for all runs $s_1 s_2 s_3 \dots$ in M such that $s = s_1$ we have $(M, s_i) \models \varphi$ for all i > 1
- $(M, s) \models \mathbf{EG} \varphi$ if for some runs $s_1 s_2 s_3 \dots$ in M such that $s = s_1$ we have $(M, s_i) \models \varphi$ for all $i \ge 1$ Taken from course notes on CTL

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CTL Semantics (Cont'd)

 $(M, s) \models \mathbf{AF} \varphi$ if for all runs $s_1 s_2 s_3 \dots$ in M such that $s = s_1$

there exists i > 1 such that $(M, s_i) \models \varphi$

 $(M, s) \models \mathbf{EF} \varphi$ if for some run $s_1 s_2 s_3 \dots$ in M such that $s = s_1$ there exists $i \geq 1$ such that $(M, s_i) \models \varphi$ $(M, s) \models \mathbf{A}[\varphi_1 \mathbf{U} \varphi_2]$ if for all runs $s_1 s_2 s_3 \dots$ in M such that $s = s_1$ there exists some $i \geq 1$ such that $(M, s_i) \models \varphi_2$, and for all $1 \leq j \leq i$, we have $(M, s_i) \models \varphi_1$ $(M, s) \models \mathbf{E}[\varphi_1 \mathbf{U} \varphi_2]$ if for some run $s_1 s_2 s_3 \dots$ in M such that $s = s_1$ there exists some $i \geq 1$ such that $(M, s_i) \models \varphi_2$, and for all $1 \leq j < i$, we have $(M, s_i) \models \varphi_1$ CISC422/853, Winter 2009 Specifying 70 CTL Examples (2) "C0 and C1 are never in their AG $!(pc_0 = cr_0 \land pc_0 = cr_0)$ critical region at the same time" "C0 will always eventually AG ($pc_0 = nc_0 \rightarrow AF pc_0 = cr_0$) be able to enter its critical region" AG $(pc_1=nc_1 \rightarrow AF pc_1=cr_1)$ turn=0urn=0 l_0, l_1 urn= l_0, nc_1 turn=1 l_0, nc_1 turn=0turn= nc_0, l_1 nco. l turn=0 turn=0 turn=1 l_0, cr_1 turn=1 nc_0, nc_1 cr_0, l_1 nc_0, nc_1 turn=0 cr_0, nc_1 nc_0, cr_1 CISC422/853, Winter 2009 Specif

CTL Examples (1)



· · · ·	CTL Equivalences		CTL	. Equivalences (Cont'd)
 ¬AGφ ↔ ¬EGφ ↔ ¬AFφ ↔ 	EF¬φ AF¬φ EG¬φ	Dualities	• EGφ • AFφ • EFφ	 → ¬ (AF¬ varphi) → A[tt U φ] → E[tt U φ]
$ \begin{array}{ccc} & \neg EF\phi & \leftrightarrow \\ & \neg AX\phi & \leftrightarrow \\ & \neg EX\phi & \leftrightarrow \end{array} $	ΑG¬φ ΕΧ¬φ ΑΧ¬φ		 • Α[φ₁ U φ₂] 	$\rightarrow \neg(E[\neg \varphi_2 U (\neg \varphi_1 \land \neg \varphi_2)] \lor EG \neg \varphi_2)$
 AGφ ↔ EGφ ↔ 	φ ∧ AX AGφ φ ∧ EX EGφ	"Unwindings"		
$\begin{array}{ccc} \bullet & AF\phi & \leftrightarrow \\ \bullet & EF\phi & \leftrightarrow \\ \bullet & A[\phi_1 \ U \ \phi_2] & \leftrightarrow \end{array}$	$\label{eq:phi} \begin{split} \phi &\vee AX \; AF \phi \\ \phi &\vee EX \; EF \phi \\ \phi_2 &\vee (\phi_1 \wedge AX \; A [\phi_1 \; U \; \phi_2]) \end{split}$			
• $E[\phi_1 \cup \phi_2] \leftrightarrow$ 3C422/853, Winter 2009 \$	$\phi_2 \lor (\phi_1 \land EX E[\phi_1 \cup \phi_2])$	73	CISC422/853, Winter 2009	Specifying

CTL vs LTL

- LTL: execution sequences are linear
- CTL: execution sequence are branching
- The two logics are incomparable wrt their expressiveness
 - There are CTL formulas that are not expressible in LTL $^\circ\,$ e.g., AF AG p
 - + There are LTL formulas that are not expressible in CTL $^\circ\,$ e.g., F G p
- Also, as we will see the algorithm for CTL model checking will be quite different from the LTL model checking algorithm that we have seen (more on this later)

Specification Patterns: Motivation

- Have already seen one way to classify properties:
 - safety
 - liveness
- This classification is very useful, because it impacts
 - design of analysis algorithms
 - design of optimization algorithms
 - use of existing tools (e.g., Spin)
- However, it's also very coarse

Specification Patterns: Motivation (Cont'd)

- Lots of interesting properties can be expressed in temporal logic
- However, as soon as temporal operators are nested, formulas can become very difficult to design and read
- Example:

[]((Q ∧ []((Q & !R & <>R) -> (P -> (!R U (S & !R))) U R) "P triggers S between Q and R"

 Would be great to have a more high-level way to think of temporal properties

$\neg R \land {\boldsymbol{<>}}R) \ \to \ (P \to (\neg R \ U \ (S \land \neg R))) \ U \ R)$	_
or in ASCII format	-

- Developed by Dwyer, Avrunin, and Corbett Pattern system for presenting, codifying, and reusing
- property specifications for finite-state verification

Specification Pattern System

- similar to Design Patterns in OO Programming
- Developed by examining over 500 temporal specifications collected from the literature
- Organized into a hierarchy based on the semantics of the requirement
- http://patterns.projects.cis.ksu.edu

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Specification Patterns: Example



Specification Patterns: Example (Cont'd)





Specification Patterns: Hierarchy (Cont'd)

- Absence
 - · A state/event does not occur within a given scope
- Existence
 - · A state/event must occur within a given scope
- Bounded existence
 - A state/event must occur {at most, exactly, at least} k times within a given scope
- Universality
 - · A state/event does occur throughout a given scope
- Precedence
 - · A state/event P must always be preceded by a state/event Q
- Response

A state/event P must always be followed by a state/event Q
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Specification Patterns: Examples in LTL

Pattern Mappings

<u>Absence</u>

P is false :

Globally	[](!P)			
Before R				
After Q	[](Q -> [](!P))	Σ	Scor	hes
Between Q and R	[]((Q & !R & ⇔R) → (!P U R))		000	
(*) After Q until R	[](Q & !R -> (!P W R))			

Existence

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P becomes true :

Globally	⇔(P)
(*) Before R	!R W (P & !R)
After Q	$[](!Q) \Leftrightarrow (Q \mathrel{\mathrel{\scriptstyle{\triangleleft}}} \Leftrightarrow P))$
(*) Between Q and R	[](Q & !R -> (!R W (P & !R)))
(*) After Q until R	[](Q & !R -> (!R U (P & !R)))

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Specification Patterns: Examples in LTL (Cont'd)

<u>Response</u>

S responds to P :

Globally	[](P → ⇔S)
(*) Before R	<pre><>R -> (P -> (!R U (S & !R))) U R</pre>
After Q	$[](Q \rightarrow [](P \rightarrow \Diamond S))$
(*) Between Q and R	$\label{eq:rescaled} \fbox{$((Q \& !R \& \diamondsuit R) \rightarrow (P \rightarrow (!R U (S \& !R))) U R)]}$
(*) After Q until R	[](Q & !R -> ((P -> (!R U (S & !R))) W R)

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